CLAIMS

I claim:

1. A process of fabricating a power MOSFET comprising:

providing a substrate of a first conductivity type;

providing an epitaxial layer of a second conductivity type opposite to said first conductivity type on the substrate;

forming a trench in the epitaxial layer;

implanting dopant of said first conductivity type through a bottom of the trench to form a drain-drift region beneath said trench and within said epitaxial layer, immediately following said implanting said drain-drift region extending from said trench to said substrate;

forming an insulating layer along the bottom and a sidewall of the trench;

introducing a conductive gate material into the trench; and

introducing dopant of the first conductivity type into the epitaxial layer to form a source region, the drain-drift region and the source region being formed under conditions such that the source region and drain-drift region are separated by a channel region of the epitaxial layer adjacent the sidewall of the trench.

2. The process of Claim 1 wherein providing an epitaxial layer comprises growing an epitaxial layer of the second conductivity type on the substrate.

3. The process of Claim 1 wherein providing an epitaxial layer comprises growing an epitaxial layer of said first conductivity type and implanting dopant of a second conductivity type opposite to said first conductivity type into said epitaxial layer.

4. The process of Claim 3 comprising heating said epitaxial layer so as to diffuse said dopant of said second conductivity type to an interface between said epitaxial layer and said substrate.

5. The process of Claim 1 comprising implanting dopant of said second conductivity type into said epitaxial layer to form a body region.

6. The process of Claim 7 wherein implanting dopant of said first conductivity type through a bottom of the trench to form a drain-drift region comprises implanting dopant at an energy of from 100 keV to 2.0 MeV.

7. A process of fabricating a power MOSFET comprising:

providing a substrate of a first conductivity type;

providing an epitaxial layer of a second conductivity type opposite to said first conductivity type on the substrate;

forming a trench in the epitaxial layer;

implanting dopant of said first conductivity type through a bottom of the trench to form a region of dopant beneath said trench and within said epitaxial layer, said region of dopant being located above and separated from said substrate;

heating said substrate so as to cause said region of dopant to diffuse downward so as to form a drift-drain region extending from said bottom of said trench to said substrate;

forming an insulating layer along the bottom and a sidewall of the trench;

introducing a conductive gate material into the trench; and

introducing dopant of the first conductivity type into the epitaxial layer to form a source region, the drain-drift region and the source region being formed under conditions such that the source region and drain-drift region are separated by a channel region of the epitaxial layer adjacent the sidewall of the trench.

8. The process of Claim 7 wherein providing an epitaxial layer comprises growing an epitaxial layer of the second conductivity type on the substrate.

9. The process of Claim 7 wherein providing an epitaxial layer comprises growing an epitaxial layer of said first conductivity type and implanting dopant of a second conductivity type opposite to said first conductivity type into said epitaxial layer.

10. The process of Claim 9 comprising heating said epitaxial layer so as to diffuse said dopant of said second conductivity type to an interface between said epitaxial layer and said substrate.

11. The process of Claim 7 comprising implanting dopant of said second conductivity type into said epitaxial layer to form a body region.

12. The process of Claim 7 wherein implanting dopant of said first conductivity type through a bottom of the trench to form a region of dopant comprises implanting dopant at an energy of from 30 keV to 300 keV.

13. A process of fabricating a power MOSFET comprising:

providing a substrate of a first conductivity type;

providing an epitaxial layer of a second conductivity type opposite to said first conductivity type on the substrate;

forming a trench in the epitaxial layer;

implanting dopant of said first conductivity type through a bottom of the trench to form a deep layer of dopant beneath said trench and approximately at an interface between said substrate and said epitaxial layer, said deep layer of dopant being located below and separated from said trench;

heating said substrate so as to cause said deep layer of dopant to diffuse upward so as to form a drift-drain region extending from said bottom of said trench to said substrate;

forming an insulating layer along the bottom and a sidewall of the trench;

introducing a conductive gate material into the trench; and

introducing dopant of the first conductivity type into the epitaxial layer to form a source region, the drain-drift region and the source region being formed under conditions such that the source region and drain-drift region are separated by a channel region of the epitaxial layer adjacent the sidewall of the trench.

14. The process of Claim 13 wherein providing an epitaxial layer comprises growing an epitaxial layer of the second conductivity type on the substrate.

15. The process of Claim 13 wherein providing an epitaxial layer comprises growing an epitaxial layer of said first conductivity type and implanting dopant of a second conductivity type opposite to said first conductivity type into said epitaxial layer.

16. The process of Claim 15 comprising heating said epitaxial layer so as to diffuse said dopant of said second conductivity type to an interface between said epitaxial layer and said substrate.

17. The process of Claim 13 comprising implanting dopant of said second conductivity type into said epitaxial layer to form a body region.

18. The process of Claim 13 wherein implanting dopant of said first conductivity type through a bottom of the trench to form a deep layer of dopant comprises implanting dopant at an energy of from 300 keV to 3.0 MeV.

19. A process of fabricating a power MOSFET comprising:

providing a substrate of a first conductivity type;

providing an epitaxial layer of a second conductivity type opposite to said first conductivity type on the substrate;

forming a trench in the epitaxial layer;

implanting dopant of said first conductivity type through a bottom of the trench to form a deep layer of dopant beneath said trench and approximately at an interface between said substrate and said epitaxial layer;

implanting dopant of said first conductivity type through a bottom of the trench to form a region of dopant beneath said trench and within said epitaxial layer, said region of dopant being located above and separated from said deep layer of dopant;

heating said substrate so as to cause said deep layer of dopant to diffuse upward and said region of dopant to diffuse downward, said deep layer and said region merging to form a drift-drain region extending from said bottom of said trench to said substrate;

forming an insulating layer along the bottom and a sidewall of the trench;

introducing a conductive gate material into the trench; and

introducing dopant of the first conductivity type into the epitaxial layer to form a source region, the drain-drift region and the source region being formed under conditions such that the source region and drain-drift region are separated by a channel region of the epitaxial layer adjacent the sidewall of the trench.

20. The process of Claim 19 wherein providing an epitaxial layer comprises growing an epitaxial layer of the second conductivity type on the substrate.

21. The process of Claim 19 wherein providing an epitaxial layer comprises growing an epitaxial layer of said first conductivity type and implanting dopant of a second conductivity type opposite to said first conductivity type into said epitaxial layer.

22. The process of Claim 21 comprising heating said epitaxial layer so as to diffuse said dopant of said second conductivity type to an interface between said epitaxial layer and said substrate.

23. The process of Claim 19 comprising implanting dopant of said second conductivity type into said epitaxial layer to form a body region.

24. The process of Claim 19 wherein implanting dopant of said first conductivity type through a bottom of the trench to form a region of dopant comprises implanting dopant at an energy of from 30 keV to 300 keV.

25. The process of Claim 19 wherein implanting dopant of said first conductivity type through a bottom of the trench to form a deep layer of dopant comprises implanting dopant at an energy of from 300 keV to 3.0 MeV.

26. A process of fabricating a power MOSFET comprising:

providing a substrate of a first conductivity type;

growing an epitaxial layer on the substrate;

forming a trench in the epitaxial layer;

implanting dopant of said first conductivity type through a bottom of the trench to form a first region of dopant beneath said trench;

implanting dopant of said first conductivity type through a bottom of the trench to form a second region of dopant beneath said trench, said first and second regions overlapping each other immediately after said implanting, said first and second regions being arranged in a stack extending between said trench and said substrate;

forming an insulating layer along the bottom and a sidewall of the trench;

introducing a conductive gate material into the trench; and

introducing dopant of the first conductivity type into the epitaxial layer to form a source region, the drain-drift region and the source region being formed under conditions such that the source region and drain-drift region are separated by a channel region of the epitaxial layer adjacent the sidewall of the trench.

27. The process of Claim 26 where said substrate is not subjected to any substantial thermal processing after said implanting of dopant to form said first and second regions.

28. A process of fabricating a power MOSFET comprising:

providing a substrate of a first conductivity type;

growing an epitaxial layer on the substrate;

forming a trench in the epitaxial layer;

implanting dopant of said first conductivity type through a bottom of the trench at a plurality of predetermined energies to form a plurality of dopant regions of dopant beneath said trench, immediately after said implanting adjacent ones of said dopant regions overlapping so as to form a stack extending between said trench and said substrate;

forming an insulating layer along the bottom and a sidewall of the trench;

introducing a conductive gate material into the trench; and

introducing dopant of the first conductivity type into the epitaxial layer to form a source region, the drain-drift region and the source region being formed under conditions such that the source region and drain-drift region are separated by a channel region of the epitaxial layer adjacent the sidewall of the trench.

29. A power MOSFET comprising:

a substrate of a first conductivity type;

an epitaxial layer on said substrate, said epitaxial layer generally being of a second conductivity type opposite to said first conductivity type, a trench being formed in said epitaxial layer;

an insulating layer lining a bottom and a sidewall of said trench;

a conductive gate in said trench;

a source region adjacent a surface of said epitaxial layer; and

a drain-drift region of said first conductivity type extending through said epitaxial layer from a bottom of said trench to said substrate, said drain-drift region forming a PN junction with a portion of said epitaxial layer of said second conductivity type.

30. The power MOSFET of Claim 29 wherein at least 75% of a cross-sectional area of said drain-drift region is located directly below said trench.

31. The power MOSFET of Claim 30 wherein at least 90% of a cross-sectional area of said drain-drift region is located directly below said trench.

32. The power MOSFET of Claim 29 wherein said PN junction intersects a sidewall of said trench.

33. The power MOSFET of Claim 29 wherein said PN junction is concave in the towards an interior portion of said drain-drift region.

34. The power MOSFET of Claim 29 wherein said drain-drift region comprises a plurality of implants made at different energies.

35. The power MOSFET of Claim 29 wherein said epitaxial layer comprises two sublayers having different doping concentrations.

36. The power MOSFET of Claim 29 comprising a body region of said second conductivity type in said epitaxial layer.

37. The power MOSFET of Claim 36 wherein a lower border of said body region is at a level below a bottom of said trench.

38. The power MOSFET of Claim 37 wherein said body region extends to said substrate.

39. A power MOSFET comprising:

a substrate of a first conductivity type;

an epitaxial layer on said substrate, said epitaxial layer generally being of a second conductivity type opposite to said first conductivity type, a trench extending from a surface of said epitaxial layer through said epitaxial layer and into said substrate;

an insulating layer lining a bottom and a sidewall of said trench;

a conductive gate in said trench; and

a source region of said first conductivity type adjacent said surface of said epitaxial layer and a sidewall of said trench.